CPW-Fed Suspended 60 GHz On-chip Phased Array with High Efficiency

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***Abstract*—Major shortcoming of current silicon-based millimeter-wave (mmW) on-chip antennas is the low radiation efficiency (5-10%). In this paper, we propose a phased antenna array on silicon substrate with the radiation efficiency >80% at 60 GHz. This is achieved by suspending radiating elements using micro-electro-mechanical systems (MEMS) processes, thus creating a low-ϵ_r substrate of air instead of lossy silicon substrate. The designed 5×5 (element) array is well matched at 60 GHz with the -10 dB bandwidth of 2 GHz. The peak realized gain for the 5×5 array is 19.7 dBi with the gain reduction of ≤4 dB at the maximum scanning angle. Moreover, the scanning volume of the designed antenna is $\pm 45°$ in *H* plane and $\pm 48°$ in *E* plane. As an on-chip phased array, the designed array can be monolithically integrated on a silicon substrate. Moreover, unlike other arrays, it satisfies high realized gain and moderate scanning volume in both *E* and *H* planes, making it desirable for next-generation wireless systems.**

Keywords—Suspended; MEMS; On-chip Antenna; Phased Array; Millimeter Wave

I. Introduction

As the wireless applications rapidly increase, data traffic congestion becomes an issue at the traditional microwave spectrum [1]. To acquire higher data rates, the untapped millimeter-wave band has the potential for supporting 200 times more bandwidth for various wireless communication applications [2]. The 60 GHz is one of the candidates for next-generation communication systems due to available 7 GHz unlicensed band (57-64 GHz) targeting short-range communication. However, mmW frequencies pose several challenges. For example, the signal propagation is impaired by severe path-loss at mmW frequencies [3]. In addition, it is important to be directive for mobile applications in case that the transmitters or receivers are moving. Therefore, it is important to optimize mmW antenna arrays to be capable of scanning with high realized gain.

The major problems of mmW antennas-utilized for direct integration on chip-is low radiation efficiency (5-10%) and consequently low realized gain [4]. For this approach, the radiating antenna is located on the substrate resulting in low radiation efficiency. Because the ratio of radiated power to the total power decreases as the dielectric constant of the substrate increases [5]. For instance, more than 95% of radiated power couple to silicon substrate due to high dielectric constant of 11.9.

Currently there are several approaches to increase the efficiency of on-chip antennas. For example, an on-chip ground plane is adopted to reflect the radiated power into the air [6]. For this configuration, the SiO_2 layer is placed between the antenna and the substrate. It is important to note that the height of this SiO_2 layer impacts the antenna-to-ground coupling and determines the radiation resistance. However, this finite height is limited due to fabrication requirements, thus decreasing the radiation resistance. As a result, the radiation efficiency is less than 45% due to ohmic losses. In addition, an off-chip ground layer is implemented underneath the silicon substrate. Due to high dielectric constant and large height of silicon substrate, most of power couples into surface-wave modes, thus the radiation efficiency is ~10%-20% [5-6].

In this paper we present a novel on-chip 5×5 array to achieve >80% efficiency using MEMS suspended radiating elements. By suspending the patch antenna above the ground plane, the effective dielectric constant is reduced, thus decreasing the losses due to dielectric, conduction, and surface wave modes. Moreover, capacitive feeding scheme is used for the ease of fabrication and monolithic integration with T/R modules. Moreover, we have improved our previous work by designing feeding network using coplanar waveguide (CPW) feeding line rather than microstrip line feeding network [7-8], which reduces radiation loss and crosstalk. Furthermore, it simplifies fabrication and monolithic integration by eliminating the thin signal line of 1-2 μm and SiO_2 layer. In addition, the CPW-based feeding scheme can optimize the radiating patch and feeding separately. In Section II, the design and architecture of antenna array are presented. The fabrication of the phased array antenna is discussed in Section III. Finally, the scanning range in both *E* and *H* planes are analyzed and the impedance bandwidth is presented in Section IV.

II. Design

Integration of mmW phased array on silicon poses several challenges, one of them is low radiation efficiency due to the high dielectric constant of silicon. For example, a dipole antenna is implemented on the substrate, the ratio of the power radiated into air to the total power is calculated by [5]

$$\frac{P_{air}}{P_{total}} = \frac{1}{\epsilon_r^{\frac{1}{2}}} \tag{1}$$

where P_{air} and P_{total} is the radiated power into air and total power, respectively. As can be seen from the formula (1), for silicon substrate ($\epsilon_r = 11.9$), less than 5% of the power couples

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into the air and most of the power couples directly into the substrate. To address the efficiency problem, we propose a novel suspended on-chip array with high efficiency and moderate scanning volume while maintaining sufficient bandwidth.

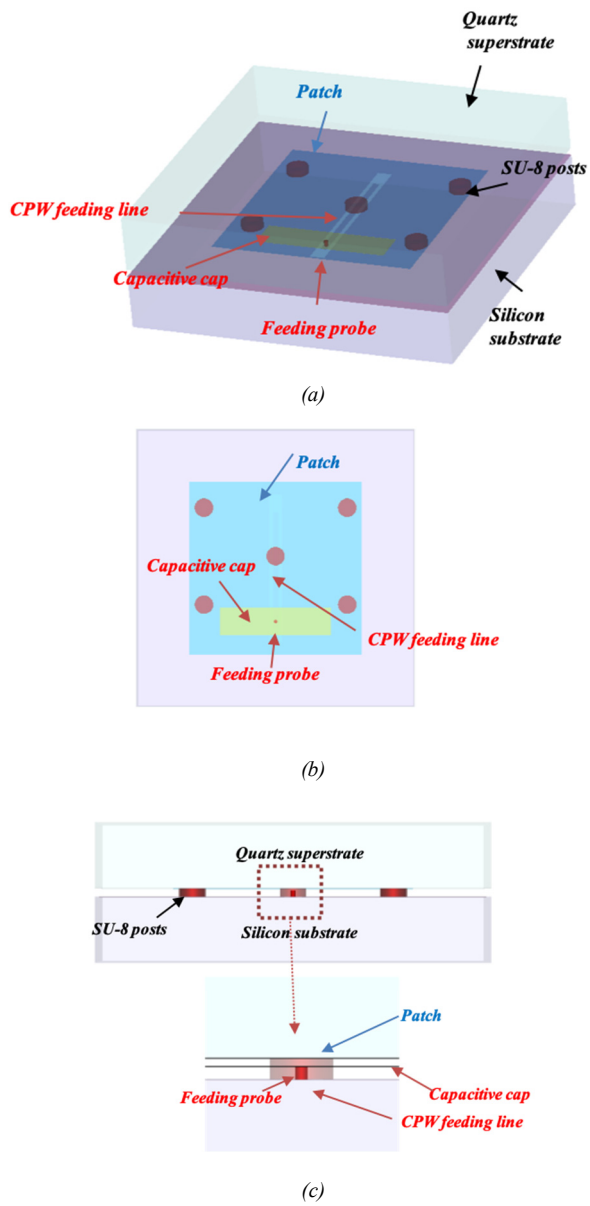

Fig.1. a) 3D view of unit-cell of proposed phased array, b) Top view schematic of unit-cell, c) Side view schematic of the unit-cell

The unit-cell of on-chip phased array is illustrated in Fig.1. The proposed architecture elevates the radiating elements (patch antennas) away from the lossy substrate, which is achieved by SU-8 epoxy posts. As can be seen, a number of SU-8 posts are employed to support the radiating patch 60 µm above the ground. As an epoxy-based negative photoresist, SU-8 polymer is used as vertical posts due to high-aspect-ratio nature [9]. Consequently, an air substrate of low-ϵ_r is designed to replace the lossy and high-ϵ_r, thus increasing the radiation efficiency.

Moreover, the CPW feeding line is chosen to decrease radiation loss and crosstalk compared to microstrip line [10]. As a result, the 3-µm-thick SiO_2 layer is eliminated for easier fabrication. Moreover, the uniplanar scheme is capable of optimizing the radiating patch antenna and feeding network separately. As shown in Fig.1, the ground plane of CPW is used as the ground plane for the patch antenna. Therefore, the CPW network is located on the silicon substrate, while the radiating patch antenna is elevated on the air.

In addition, the radiating patch is fed using capacitive coupling with another feeding cap, which is supported by the 40-µm-thick probe. It is important to note that this feeding probe is fabricated by metallization of inner SU-8 post. For capacitive coupling, the distance between the radiating patch and feeding cap determines the suitable mode for patch antenna, which is also optimized for impedance matching and efficiency analysis. Furthermore, capacitive feeding simplifies the fabrication process by dividing the architecture into two wafers, which can be fabricated separately and bonded for final design.

Moreover, as can be seen from Fig.2, the array is 5×5 (12.5 mm×12.5 mm), which is chosen for ease of measurement. The element spacing is 2.5 mm which is half the free space wavelength at 60 GHz. Each array element is fed with a T/R module, which is suitable for active scanning arrays.

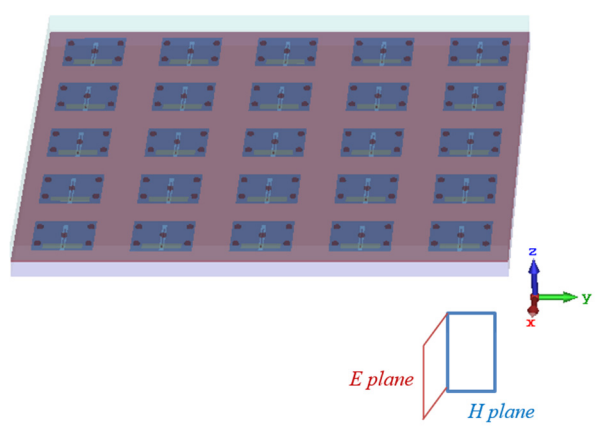

Fig.2. 3D view of the proposed 5×5 phased array

III. Fabrication

The proposed antenna array is fabricated on a 500-µm-thick silicon wafer. First, the CPW feeding line is patterned using 1-µm-thick gold layer. A 35-µm SU-8 pin is spin coated and patterned as polymer core of feeding probe. Next, a conformal gold layer is deposited to form the feeding pin. Then a 1-µm-thick gold layer is deposited and patterned to form a capacitive feeding cap.

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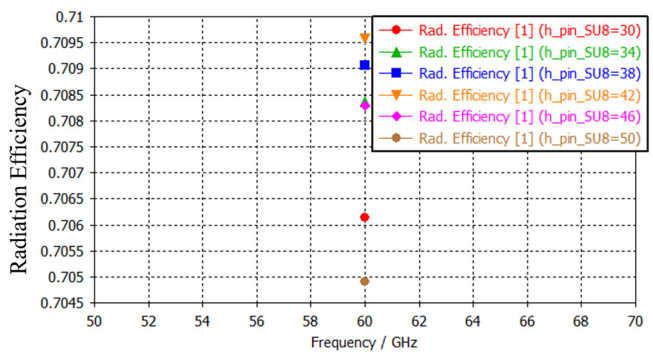
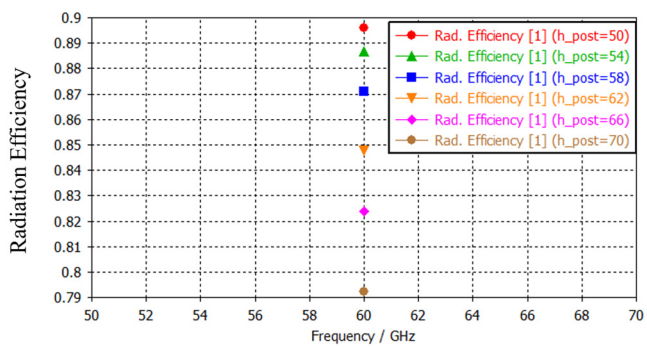
On a separate 500-µm-thick Quartz substrate, the radiating patch is deposited and etched using 1 µm gold layer. Five 60-µm-thick SU-8 supporting posts are spin coated for suspended elements. After all SU-8 posts are formed, the wafer is flipped and bonded to silicon wafer for final array structure.

IV. Results



(a)



(b)

Fig.3. Simulated radiation efficiency for unit-cell as a function of (a) feeding probe height (b) SU-8 posts height

The designed antenna array is simulated using time-domain CST Design Studio. The radiation efficiency analysis is illustrated in Fig.3. As two important parameters for capacitive coupling, the height of feeding pin and SU-8 posts are optimized to increase the radiation efficiency. It is important to observe that the height of SU-8 posts impact the efficiency significantly, while the height of feeding pin has little impact on the efficiency.

As shown in Fig. 4, the -10 dB impedance bandwidth of the designed array is 2 GHz, which is sufficient for most 60 GHz applications. Fig.5 shows the realized gain at *E* plane and *H* plane, respectively. As can be observed, the realized gain is 19.7 dBi with side-lobe level of -13 dB for broadside scanning. Moreover, this 5×5 antenna array is capable of ±45° scanning in *H* plane and ±48° scanning in *E* plane. It is important to note that the gain reduction is less than 4 dB for maximum scanning angle, i.e., the designed array shows high realized gain considering all scanning angles. The radiation efficiency of the phased array is calculated as 85%. Detailed fabrication process, together with antenna scanning analysis and measurements will be presented at the conference.

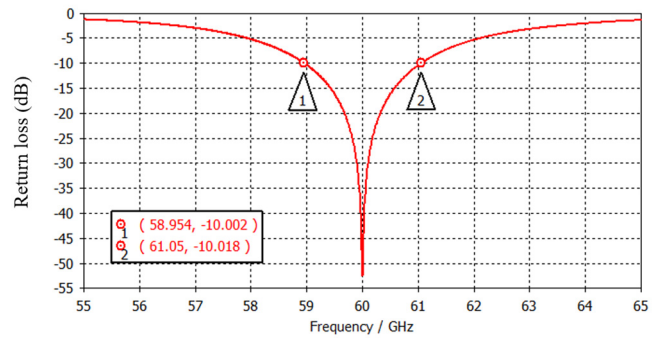


Fig.4. Simulated S_{11} of the center element of the 5×5 array at broadside scanning showing that -10 dB bandwidth is 2 GHz.

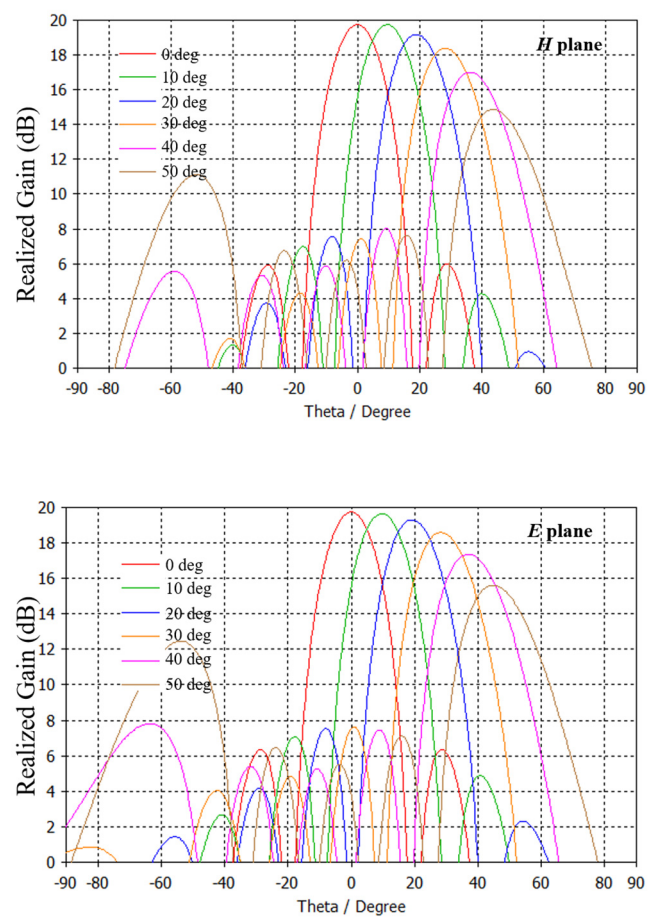


Fig.5. Simulated *H-Plane* (top) and *E-Plane* (bottom) radiation patterns (realized gain) of the 5×5 array as a function of scanning angle (0° to 50° with steps 10°) at 60 GHz.

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V. Conclusion

In this paper we presented a novel design to increase the radiation efficiency for on-chip antenna arrays at 60 GHz. To overcome the low radiation efficiency (~5-10%) due to lossy substrate, we proposed a phased array on silicon substrate with the radiation efficiency >80% at 60 GHz. This is achieved by MEMS suspension, thus creating a low-ϵ_r substrate of air rather than lossy silicon substrate. The designed 5×5 array is well matched with the -10 dB bandwidth of 2 GHz. The peak realized gain for the 5×5 array is 19.7 dBi with -13 dB sidelobes level. Moreover, the scanning volume of the designed antenna is $\pm 45°$ in *H* plane and $\pm 48°$ in *E* plane. Compared with other mmW arrays, the designed array satisfies the high radiation efficiency and moderate scanning volume in both *E* and *H* planes, which is desirable for next-generation wireless systems.

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