VCSEL Scaling, Laser Integration on Silicon, and Bit Energy

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Abstract: A new VCSEL is described to scale to smaller lasers for high speed, integration, and low bit energy optical interconnects.

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Introduction:

Future scaling for on-chip optical interconnects will depend heavily on which optoelectronic technology can produce the lowest bit energy. We show in this paper that a significant influence on bit energy will be the modulation scheme that is used, and especially the laser. Highly compact directly modulated lasers (DMLs) have been researched to meet this goal. The most favored technology will likely be set by how it impacts bit energy, and this bit energy must be achieved at usable temperatures such as 0 to 85 C, or even 0 to 100 C. The combined need of high efficiency with high temperature operation eliminates essentially all laser diode technologies except VCSELs. Therefore scaling of the VCSEL and on-chip integration schemes that can take advantage of the scaled VCSEL approach and the compact laser footprint.

There is also the question of which achieves lower bit energy, a DML or a continuous-wave (CW) laser coupled to an integrated modulator. Transceiver suppliers are also recognizing that for short distances VCSELs will maintain their bit energy and cost advantages over existing silicon photonics. The bit energy advantage comes from comparing a directly modulated laser with small active volume (VCSEL) with a less efficient continuous-wave laser with ten times the active volume, and that suffers further loss of efficiency due to optical couplings and the optical modulator requirement. To add to the technical advantage of its lower bit energy, VCSEL transceivers can be assembled with much lower cost than silicon photonics again for fundamental reasons. High volume costs of silicon photonics will be limited by how it fabricates its laser, just like for VCSELs. VCSELs use lower cost III-V materials and can be made with lower cost than silicon photonic lasers. VCSEL scaling for on-chip integration for optical interconnects follows this path of development that can utilize high efficiency DMLs that reach very high modulation speed.

Oxide-VCSELs [1] do not yet take full advantage of the volume and cost benefits of using a high-speed small cavity laser for on-chip optical interconnects, and have manufacturing difficulties in device scaling to very small size. New VCSEL technology is described in this paper that promises continued scaling in semiconductor laser volume [2]-[5] for increase in direct modulation and integration into various platforms. Many of the largest VCSEL applications include data centers and high performance computers. Although silicon photonics has also been proposed and demonstrated for optical links, at short distances VCSELs continue to be used as the transceiver laser of choice because of its lower bit energy and lower cost than silicon photonics.

In this paper we analyze and contrast different laser solutions for future optical interconnects, and introduce the new type of VCSEL that continues the scaling trends introduced by oxide VCSELs as well as connect to silicon photonics. Issues of efficiency, reliability, and speed will also be presented.

VCSEL Bit Energy vs. Silicon Photonics:

Figure 1 shows the electronic circuitry and comparison key to analyzing photonic bit energies for transceivers used in data centers, HPCs, and other optical switches and interconnects. A silicon photonics solution is shown in the upper diagram and a DML VCSEL solution is shown in the lower diagram of Fig. 1. The silicon photonic solution at present uses a CW laser that is either a 1550 nm or 1310 nm DFB or DBR laser coupled through a waveguide to a modulator. The DML VCSEL is coupled directly to a waveguide. These solutions will be analyzed and compared in the presentation. However it is clear that unless the CW laser is sufficiently efficient to compensate for optical losses in the interconnections, power lost in modulation, and modulator power, the DML VCSEL will produce lower bit energy. In contrast, the CW laser is significantly less efficient than the existing oxide VCSELs. The high speed combined with small cavity volume of the DML VCSEL cannot be matched with existing 1310 or 1550 nm CW lasers. Splitting the CW output of the laser using coupled waveguides increases bit energy since this adds to the optical losses.

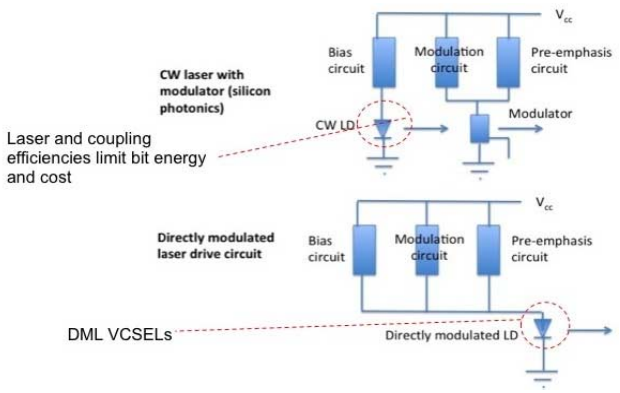

Figure 1 Upper diagram circuitry shows the case for a transmitter for silicon photonics using a CW laser diode and separate modulator. Lower diagram circuitry shows the case for a DML VCSEL. The small gain volume and high speed modulation enable lower bit energy using the DML VCSEL.

In the case of the CW laser and modulator, bit energy can be decreased by continually increasing the speed of the modulator. However the CW laser that is needed for the modulator appears to create a technological roadblock for laser diode platforms that use edge-emitting or hybrid lasers integrated onto the chip. The power consumption of the CW laser is simply too high. Comparing for example the bit energy contribution of a CW laser connected to a modulator with a DML VCSEL, the DML VCSEL wins out in bit energy for reasonable data speeds. This is because at 85 C the CW laser may consume 50 mW or more of electrical power. At a speed of 50 Gbps the laser contributes a pJ of bit energy, which is nearly 10x greater than current VCSELs. However for equivalent optical bit energy delivered to a waveguide the contribution of the CW laser and modulator are much greater due to modulation and coupling losses.

Lithographic VCSEL and Bit Energy:

The lithographic VCSELs are a new type of laser that enables scaling of the laser cavity to smaller volume than commercially available lasers, while solving manufacturing and reliability problems associated with oxide VCSELs [1]-[5]. The new lasers produce high efficiency even for micron sized laser diameter, along with excellent thermal properties. The combined enable the lithographic VCSEL to reach high efficiency in small cavity format. The thermal properties promise advances in high speed modulation by producing high intrinsic response due to very high current drive.

Figure 2 shows L-I and efficiency curves for a 2 µm diameter lithographic VCSEL. The bias current of 32 kA/cm^2 shown by the yellow vertical line is a current density needed to reach small signal intrinsic speed of more than 80 GHz, enough to exceed 100 Gbps data rate. Bit energy would be less than 5 fJ for data speed of 50 Gbps, speeds that have already been achieved for oxide VCSELs.

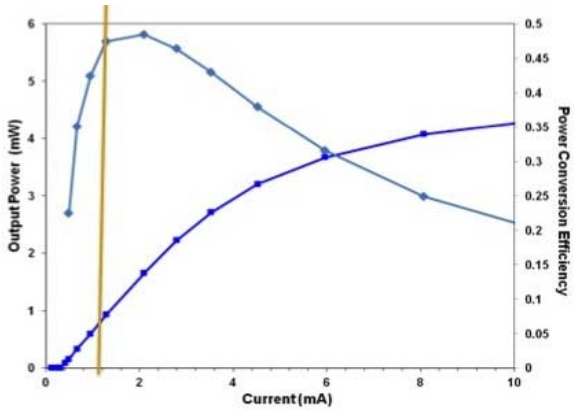

Figure 2 L-I and efficiency curves for a 2 µm diameter lithographic VCSEL. The vertical marker shows the bias current of only 1 mA is needed to reach > 30 kA/cm2 bias (high speed bias condition). Bit energy for operation at 50 Gbps, now achieved with oxide VCSELs, is projected to be less than 5 fJ.

The intrinsic response of the lithographic VCSEL is expected to enable small signal modulation beyond 100 GHz. However electrical parasitics must also be controlled and enable these speeds. The lithographic VCSELs ability to be scaled to small size also promise low electrical parasitics. These results show that continued VCSEL scaling and increasing speed will continue to reduce the bit energy of transceivers, and that existing silicon photonics will not be able to match these values. On-chip integration can include high density arrays of optical interconnects to improve chip speed.

Integration of DML VCSEL into silicon photonic platform:

The need for high operating temperature eliminates many of the possible avenues that have been attempted for silicon integration. The VCSEL however is one of the lasers for which continued scaling is possible and yet very high quality lasing can be achieved at the needed operating temperatures. Lithographic VCSELs have been demonstrated to reach efficiencies over 30 % for 1-micron diameter cavities, and operating temperatures are over 100 C.

Figure 3 shows the L-I-V characteristics for a 1 µm diameter lithographic VCSEL. On the bottom is shown a metallized and deeply etched VCSEL being studied for lift-off. Figure 3 makes clear that the technology can be used to make extremely small footprint lasers, and yet that operate as high quality lasers. The small active volume combined with the laser geometry to set what is arguably the smallest footprint possible yet for a high quality laser diode. Once fully developed footprints of 5 µm diameter or less could well be possible. Figure 4 shows an integration scheme for a very small cavity VCSEL integrated onto silicon.

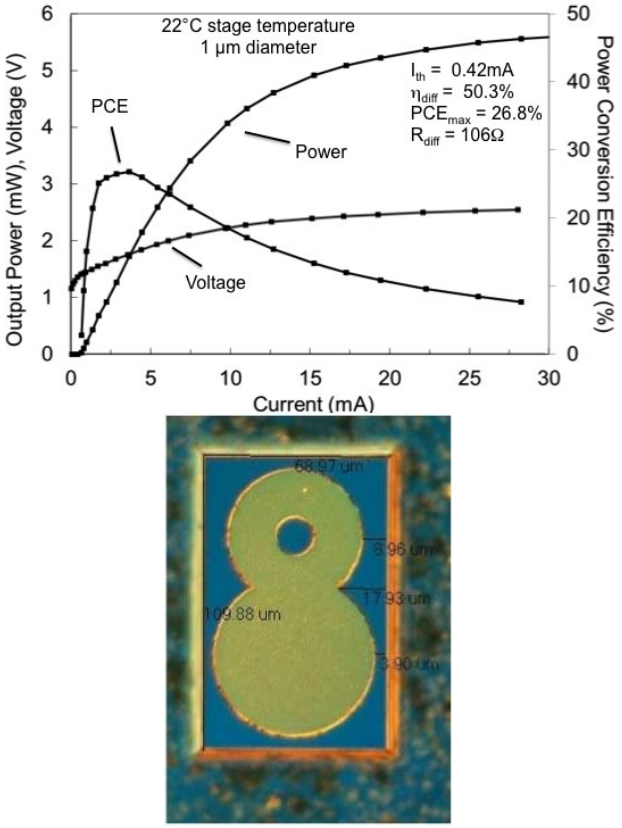

Figure 3 Above shows the L-I-V curves for a 1 µm diameter VCSEL delivering more than 5 mW of CW power. Below is shown a deeply etched lithographic VCSEL with a large Au metal contact pad. With similar etching the laser footprint may be reduced to ≤ 5 µm diameter for transferring to silicon.

The VCSEL may radiate into free space or be coupled to an on-chip waveguide such as SiN. Figure 4 shows a scheme to provide good thermal contact to the VCSEL, reduce its footprint through use of a bottom emitter with lift-off, and obtain lithographic alignment to the VCSEL aperture. A 45° micro-mirror is shown for coupling to the waveguide, however this may also be replaced by a grating. Clearly fabrication and mode coupling are important considerations in coupling efficiency. Ideally the VCSEL mode will be the size of the coupling element, and will be quite small for most waveguides of interest. For example a 1 µm tall waveguide with a 45° turning mirror will produce a horizontal aperture to the waveguide and vertical to the VCSEL to receive the laser light, of ~1.4 µm. Multimode waveguides can be considered in the horizontal or vertical dimensions, and will also influence detector design. Multimode waveguides can provide some feedback isolation to the VCSEL.

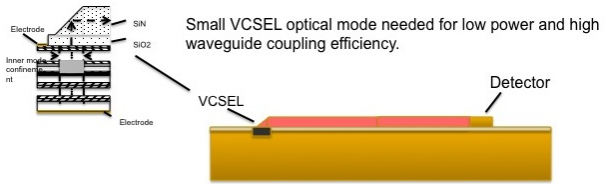

Figure 4 Schematic illustration of a VCSEL embedded into an SOI wafer with a 45° turning mirror for coupling to a SiN waveguide. A grating coupler may also be used. Various schemes may be considered for the integration, and the key enabler is the very small footprint that can be achieved with the lithographic VCSEL technology.

Conclusions

The lithographic VCSEL may provide the next generation of VCSEL scaling to reach the size, efficiency, and speed needed for dense integration into laser arrays and onto other platforms. Silicon photonics is one of these platforms that includes desirable features for both on-chip and off-chip optical interconnects. The silicon photonics approach may enable more compact chips including high performance lasers and the electronic drivers. The close coupling between lasers and electronics may increase the laser speed. Integration approaches are proposed that include mounting a lithographic VCSEL partially submerged under an oxide layer of a silicon-on-insulator wafer, to achieve low thermal resistance to the laser and a compact footprint.

Acknowledgements

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